REMARKS

Applicants request entry of this Amendment on the grounds that it places the application in condition for allowance and/or in better condition for appeal.

Applicants acknowledge the allowance of claims 1, 2, and 4.

As requested by the Examiner, the current status of U.S. application serial number 10/016,183 is provided to the Cross-Reference to Related Applications section. Additionally, Figure 10 is re-submitted with the words "New Sheet" (instead of "New Page") in the top margin thereof.

In an Office action mailed 15 July 2004, claims 3, 5, and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Stinson et al. (U.S. Pat. No.: 6,553,545) in view of Durham et al. (U.S. Pat. No.: 6,532,574). Specifically, in rejecting each of claims 3, 5, and 6, the Examiner stated:

> As per claim 3, Stinson et al. (Abstract, col. 2, lines 40 – 50, 55 – 60, col. 3, lines 15 – 21) disclose a test circuit operable to produce a signal for determining an operating reference signal. It appears though that Stinson et al. does not clearly disclose another test circuit operable to produce a signal for determining an effect of power supply noise on a signal propagation delay within a plurality of components. However, Durham et al. (col. 1, lines 25 – 37, col. 8 lines 8 – 23) teach this excepted feature. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of Durham et al. to the invention of Stinson et al. as specified above because as taught by Durham et al. (col. 1 lines 26 – 29) some common forms of noise are power supply droop and localized power variations, signal line coupling, and Miller effect capacities across circuit inputs/outputs.

Applicant filed a Response and Amendment on 25 August 2004 addressing this rejection of claims 3, 5, and 6 (among others). In the instant Office action, the Examiner stated:

> Applicant's arguments filed 8-25-04 have been fully considered by they are not persuasive with respect to the claims that remain rejected above. With respect to the arguments concerning the 35 U.S.C. 103 rejections and specifically Durham et al., the Applicant refers to Signal 1 – Signal 3 in Figures 2A – 2B as well as col. 7 lines 23 – 26, 31 – 38. However, none of these cited sections were used from the Durham et al. reference in the 35 U.S.C. 103 rejections but rather <u>what was applied from Durham et al. reference,</u> as shown in paragraph 8 of the prior Office action, were **col. 1 lines 25 – 37 and col. 8 lines 8 – 23** and no arguments were presented with respect to these applied sections of the Durham et al. reference. [Emphasis in the original.]

Although not directly referring to the sections cited by the Examiner in the previous Office action (i.e., column 1, lines 25 – 37 and column 8, lines 8 – 23), it is believed that Applicant's previous arguments apply to (and/or address the subject matter raised by) these sections. More specifically, column 1, lines 25 – 37 consists of information in the "Background of the Invention" section of the Durham reference which broadly sets forth that on-chip noise may cause a change in signal delay due to

capacitive coupling. It is respectfully submitted that Durham's mere recitation that on-chip noise causes an effect on signal delay fails to render claims 3, 5, and 6 obvious. In contrast, claims 3, 5, and 6 each recite a test circuit for determining these very effects.

Figure 7A depicts "a high level flow chart[s] for processes of determining and employing post-manufacture signal delay adjustments in accordance with the preferred embodiment" of the Durham reference. (See Col. 7, line 66 to col. 8, line 2.) Figure 7A is comprised of steps 702 – 718. Column 8, lines 8 – 23, which was cited by the Examiner, includes a description of steps 704 and 706. More specifically, column 8, lines 8 – 23 recites:

> The process first passes to step 704, which illustrates identifying pairs of adjacent signal lines within the critical path(s)--the circuit sequences constraining the timing and operational frequency--for the logic of the integrated circuit design. Although adjacent signal lines are most likely to exhibit capacitive coupling, other pairs likely to induce noise or timing delays due to capacitive coupling may also be identified and considered within this process. The process next passes to step 706, which depicts selecting a pair of the adjacent signal lines within a critical path for the integrated circuit design and determining whether any timing delays result from capacitive effects between the signal lines. This may be determined from simulations or from actual testing of integrated circuits (e.g., by comparing signal delays for rising/rising versus rising/falling signals within the adjacent signal lines).

Durham uses the actual signal lines within the critical path of the integrated circuit (not a test circuit as recited in claims 3, 5, and 6) to determine the effects of noise on signal propagation delay. More specifically, step 704 of Durham requires "identifying pairs of adjacent signal lines within the critical path(s)--the circuit sequences constraining the timing and operational frequency--for the logic of the integrated circuit design." (Column 8, lines 8 – 12.) In contrast, claims 3, 5, and 6 each recite "a test circuit operable to produce a signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components." Applicant's previous argument stated this difference. More specifically, Applicant's previous argument stated "Durham fails to disclose or teach a test circuit which produces a signal related to the effect of power supply noise on a signal propagation delay within a plurality of components." (See Page 11, Response and Amendment, filed 25 August 2005.)

Additionally, process step 706 requires "selecting a pair of the adjacent signal lines within a critical path for the integrated circuit and determining whether any timing delays result from capacitive effects between the signal lines." (Column 8, lines 16 – 19.) Applicant's previous argument stated "Durham teaches that the timing for a particular integrated circuit design is tested by loading "a dedicated scan chain ... with a default value" into the integrated circuit (col. 7, lines 31 – 32)." (See Page 11,

Response and Amendment, filed 25 August 2005.) It is respectfully submitted that this statement by Applicant (although citing to column 7, lines 31 – 32) addresses the manner in which Durham implements the step of "determining whether any timing delays result from capacitive effects between the signal lines" as recited at column 8, lines 18 – 19. Furthermore, Applicant's previous argument stated that "[t]he actual signals found on the integrated circuit's critical paths, not a signal or signals produced by a separate circuit, are then observed to determine the timing delay caused by capacitive effect (e.g., see Signal 1 – Signal 3 in FIGS. 2A – 2B)." (See Page 11, Response and Amendment, filed 25 August 2005.) It is respectfully submitted that this statement by the Applicant (although pointing to Signal 1 – Signal 3 in FIGS. 2A – 2B as an example) addresses the manner in which Durham implements the step of "selecting a pair of the adjacent signal lines within a critical path for the integrated circuit design" as recited at column 8, lines 16 – 18.

Accordingly, it is believed that Applicant's previous arguments adequately addressed the sections cited by the Examiner in the previous Office action (i.e., column 1, lines 25 – 37 and column 8, lines 8 – 23), even though Applicant's previous arguments did not directly refer to these cited sections.

Because Stinson et al. does not disclose "a test circuit operable to produce a signal for determining an effect of power supply noise on a signal propagation delay within a plurality of components" and because Durham fails to provide the missing teaching, it is believed that claims 3, 5, and 6 are in condition for allowance. Thus, it is respectfully requested that the rejection of claims 3, 5, and 6 pursuant to 35 U.S.C. §103(a) be withdrawn.

Claims 8 – 10 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 8 depends from allowable base claims 1 or 5, claim 9 depends from allowable base claims 2 or 6, and claim 10 depends from allowable base claims 3 or 6. Thus for the reasons discussed above in conjunction with claims 1 – 3 and 5 – 6, it is believed that claims 8 – 10 are in condition for allowance. Accordingly, it is respectfully requested that the objections to claims 8 – 10 be withdrawn.

Applicants have made a diligent effort to place the application in condition for allowance. Accordingly, a Notice of Allowance for claims 1 – 6, and 8 – 10 is respectfully requested. If the Examiner is of the opinion that the instant application is in condition for disposition other than through allowance, the Examiner is respectfully requested to contact applicants' attorney at the telephone number listed below so that additional changes may be discussed.

Respectfully submitted,

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Amendments to the Drawings:

Figure 10, which is now identified as "New Sheet" as required by 37 C.F.R. 1.121, is re-submitted herewith. Figure 10 is added to the drawings to offer a more detailed illustration of the features of operation 903 as found in Figure 9. Support for new Figure 10 may be found in paragraphs 65 – 66. No new matter is added.